What is claimed is:

1. An arbitration circuit for arbitrating bus access requests presented from a plurality of bus masters connected through a shared bus, comprising:

a priority check block receiving multiple pieces of priority information outputted respectively from said plurality of bus masters, for comparing said pieces of priority information and specifying masters with a highest priority so as to output a check result; and

a round robin block,

said round robin block comprising,

a round robin control unit for determining, through a round robin algorithm, a priority order of the bus access requests from said plurality of bus masters,

a round robin masking unit for masking data of said check result with mask data to output a masked check result, said mask data being generated on the basis of said priority order, and

a final selection unit for selecting a bus master whose bus access request should be accepted on the basis of said masked check result and said check result.

2. The arbitration circuit according to claim 1, wherein said priority check block comprises:

a plurality of first-stage check circuits each receiving two pieces of said priority information as a set, for comparing said two pieces of priority information and outputting a higher priority information as an output priority; and

at least one next-stage check circuit receiving two, as a set, of said plurality of output priorities from said first-stage check circuits, for comparing said two output

priorities and specifying masters with a highest priority.

3. The arbitration circuit according to claim 1,

wherein said check result and said mask data are each multi-bit data in which individual bits are assigned respectively to said plurality of bus masters,

said mask data masks a bit or bits of higher-order than a bit that is assigned to a master with a highest-priority order, and

said round robin masking unit performs a logical operation with the data of said check result and said mask data to obtain said masked check result.

4. The arbitration circuit according to claim 3,

wherein the data of said masked check result and the data of said check result are given to said final selection unit as consecutive data in which the data of said masked check result forms a high-order portion and the data of said check result forms a low-order portion, and

said final selection unit searches said consecutive data from its highest-order position to find a bit position where a given logical value appears first, and determines the bus master assigned to that bit position as a bus master whose request should be accepted.

5. A data processing system having an arbitration circuit that receives multiple pieces of priority information outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests,

wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information, and

each said priority generating circuit ups the level of said priority information

when a bus access request from the corresponding bus master is unaccepted.

6. The data processing system according to claim 5, wherein each said priority generating circuit comprises a priority up circuit for, when a bus access request was unaccepted with an outputted piece of priority information, adding or subtracting a given value to or from said outputted piece of priority information, so as to set a new piece of priority information.

7. The data processing system according to claim 6, wherein each said priority generating circuit further comprises a priority changing quantity setting register for setting said given value.

8. The data processing system according to claim 6, wherein each said priority generating circuit further comprises a limiting circuit for limiting the priority upping of said priority information.

9. A data processing system having an arbitration circuit that receives multiple pieces of priority information outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests,

wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information, and

said priority generating circuit outputs one of pieces of priority information that correspond respectively to a plurality of operating frequencies.

10. The data processing system according to claim 9, wherein each said

priority generating circuit comprises a plurality of priority setting registers in which the pieces of priority information corresponding to said plurality of operating frequencies are set in advance, and

said priority generating circuit selects one of the values set in said plurality of priority setting registers and outputs the selected value as said priority information.

11. The data processing system according to claim 9, wherein said priority generating circuit comprises an adding/subtracting circuit for adding or subtracting a given value to or from reference priority information to set a new piece of priority information.

12. The data processing system according to claim 11, wherein said priority generating circuit further comprises a limiting circuit for limiting a maximum value and a minimum value of said new priority information.

13. A data processing system having an arbitration circuit that receives multiple pieces of priority information outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests,

wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information, and

when a condition of a corresponding bus master is changed, said priority generating circuit outputs one of pieces of priority information that correspond respectively to a plurality of conditions.

14. The data processing system according to claim 13, wherein each said priority generating circuit comprises a plurality of priority setting registers in which the

pieces of priority information corresponding to said plurality of conditions are set in advance, and

when the condition of said bus master is changed, said priority generating circuit selects one of the values set in said plurality of priority setting registers and outputs the selected value as said priority information.

15. The data processing system according to claim 13, wherein said plurality of conditions comprise:

a condition in which a central processing unit in said bus master has detected a branch instruction and is presenting a request for fetching an instruction from a branch destination;

a condition in which an instruction queue for said central processing unit is vacant; and

a condition in which a store buffer in said central processing unit is full and data to be stored next is waiting.